



design and verification consultants

right from the start



Advanced VMM Verification with SystemVerilog (CM102)

Advanced Level—4 days

The advanced VMM and SystemVerilog training course educates engineers with best in class verification practises. Through a set of well documented course notes and hands on practical examples, the course empowers engineers with the verification know-how and methods they require to become VMM enabled.

Who should attend?

Verification engineers who need to develop, deploy and support VMM style SystemVerilog verification environments.

Design engineers who wish to make use of VMM and SystemVerilog infrastructure.

Engineering professionals who wish to improve their knowledge of SystemVerilog.

What will you learn?

The key VMM constructs that are essential in building a VMM style SystemVerilog verification environment. The best practises in use today in designing Interface Specifications, Transactors, Scoreboards, Transaction level models (TLM's), Functional coverage models and assertions. The ability to create your own VMM style verification environment and Verification IP through design for re-use strategies.

Pre-requisites

A sound working knowledge of Verilog / VHDL code. An understanding of the principles behind Object Orientated programming techniques. An understanding of traditional verification methods based upon RTL design languages.

Course Materials

A complete set of course notes and laboratory training material. 40% of the course is based on labs.

Structure and Course Content

Day 1 VMM Test Bench Overview and VMM Constructs Explained

Day 2 VMM Transactor and Environment Design

Day 3 VMM Transaction Level Model Design (Scoreboard, Reference Model) Functional Coverage and Test Case Development

Day 4 VMM Applications, Verification Planning, Assertions & Sign off, Re-usable verification strategies (IP Development & Coverage Strategy)

Full Agenda (CM102)

VMM Test Bench Constructs

- TB Hierarchy
- VMM TB Classes
 - VMM_channel
 - VMM_env
 - VMM_log
 - VMM_notify
 - VMM_xactor
 - VMM_data
- VMM TB Flow
- Broadcasters
- Mailboxes
- Queues
- Associative memory arrays
- Data types
- Scoreboards
- Ref Models

VMM Transactor Design:

- Where to start?
- How to build it?
- Random generators
- Pin toggling

VMM Environment Design:

- Where to start?
- Modules and hierarchy
- Simulations

Transaction Level Model Design:

- Reference Model Design

Test Case Development:

- Directed Tests
- Constrained Tests
- Scenarios & Sequences
- Constraint Implementation
- Functional Coverage
 - Development
 - Analysis
- Regression Runs

Verification Applications:

- VMM Planner
- RAL
- Scoreboard Development

SystemVerilog Test Bench labs & Demonstration based upon:

- Verification IP models
- Standardised VMM TB solution
- Easy to learn solutions

For more information please visit: <http://www.chipright.com>

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