



design and verification consultants

right from the start



## Introduction to Verification with SystemVerilog (CM101)

### Introduction Level—1 day

The introduction to SystemVerilog verification course is tailored to provide an insight into the complex and ever changing IC verification space. The course provides an overview of the current verification trends in the semiconductor industry, highlighting the benefits and pitfalls that should be taken into account before choosing the path to follow for your next verification flow.

### Who should attend?

Engineering managers who envisage using SystemVerilog as part of their flows.  
Verification engineers who need to develop modern verification techniques.  
Engineering professionals who want an insight into SystemVerilog.

### What will you learn?

The principles of effective functional verification using SystemVerilog.  
The fundamental components that must be understood before developing a TB.  
The “must have” information about verification know-how to be able to make a key decision on choosing a verification technology to work with on your next chip.

### Pre-requisites

A sound working knowledge of RTL design and traditional verification activity.

### Course Materials

A set of course notes and a demonstration of an existing SystemVerilog verification environment.

### Structure and Course Content

- History and Evolution of SystemVerilog
- Object Orientated Verification Approach
  - Classes—The basics
- Verification Methodologies (VMM / OVM / UVM)
  - What, Why & How?
- Verification Fundamentals
  - Verification Strategy
    - Constrained Random Approach
    - Directed Test Case Approach
- Verification Essentials
  - Assertions
  - Interfaces
- Choosing the right Verification Solution—How?

### Full Agenda (CM101)

#### *History & Evolution of SystemVerilog:*

- Background
- Why SystemVerilog?
- The benefits

#### *Getting started:*

- SystemVerilog—what’s new?
- Object Orientated constructs
- Inheritance
- Mailboxes
- Queues
- Associative memory arrays
- Data Types
- Modules and hierarchy

#### *Introduction to Verification Methodologies:*

- VMM / OVM / UVM
- Channels
- Scoreboards
- Reference Models
- Transaction Level Models (TLM’s)
- Pattern Generators

#### *Introduction to Modern Verification Techniques:*

- Constrained Random Verification (CRV)
- Directed Testing (DT)

#### *Introduction to Verification Fundamentals:*

- Interfaces
- Functional Coverage
- Regressions
- Assertions

#### *SystemVerilog Test Bench Demonstration:*

- Block Level Example
- System Level Example

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